

LCFC Confidential


HS45A/HS55A(NMD461) MB Schematics Document

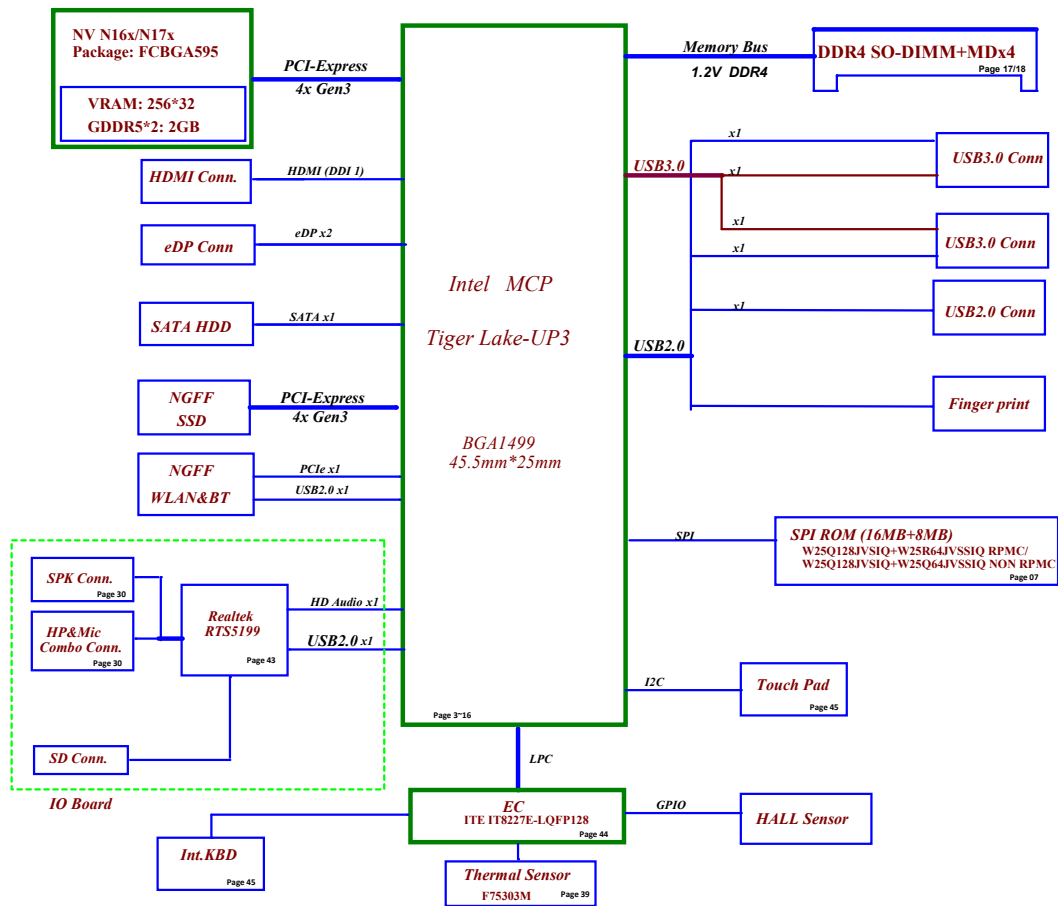
TGL UP3 with DDR4

2020-04

REV: 0.1

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page	
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				HS45A/HS55A	0.1
Date				Monday, November 12, 2018	Sheet 1 of 88





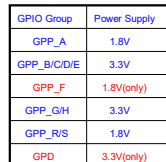
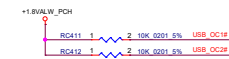
Power Plane / State	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VS +3VS +1.8VS +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X


HSIO PORT		Function
USB3.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	
	6	
USB2.0	1	USB3.0 Conn
	2	USB3.0 Conn
	3	NC
	4	NC
	5	Camera
	6	Touch Screen
	7	Finger Print
	8	Card Reader
	9	USB2.0 conn
	10	Bluetooth
PCIE	5-8 X4	DGPU
	9	WLAN
	10	NC
	11	SATA HDD
	12	NC
	13-16 X4	PCIE/SATA SSD

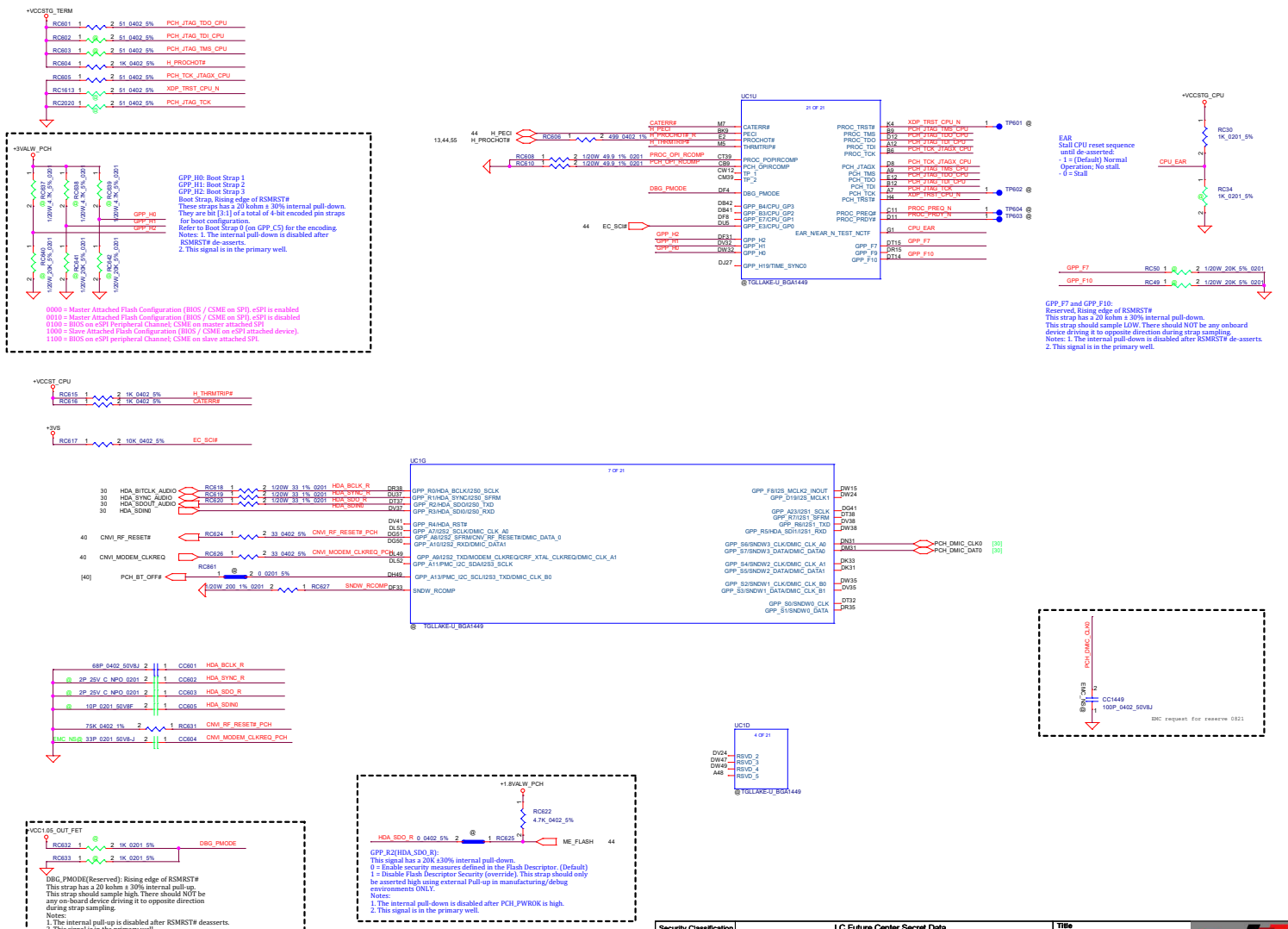
SMBUS Control Table

EC SMBus1 address		EC SMBus2 address		EC SMBus3 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100ab	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	DGPU	need to update				

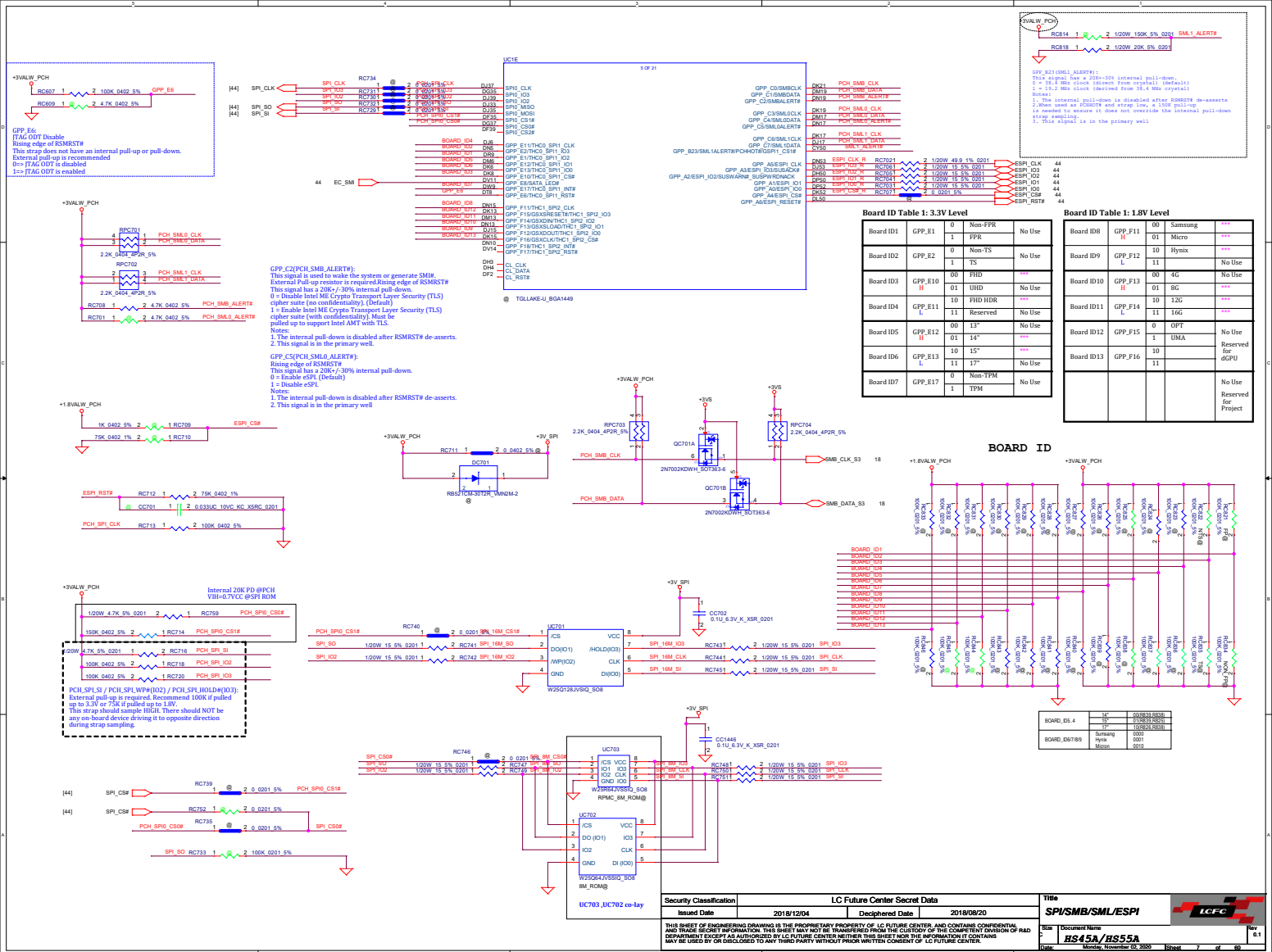
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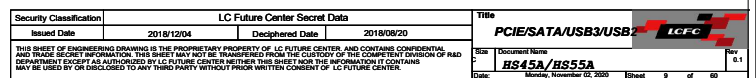


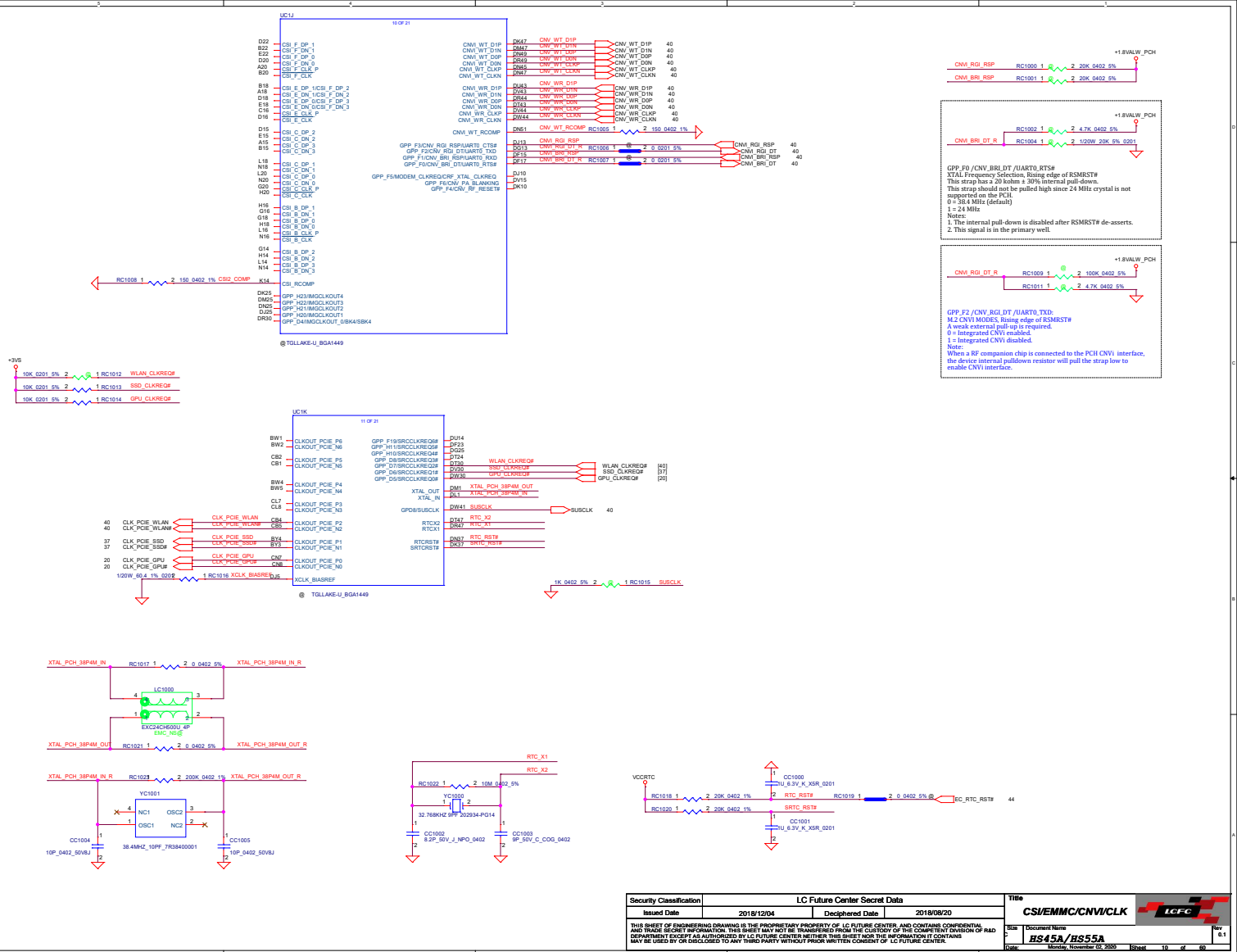
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Date			Month			Year			
						BS45A/BS55A			

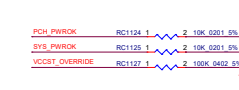
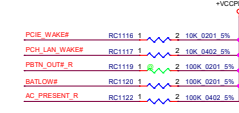
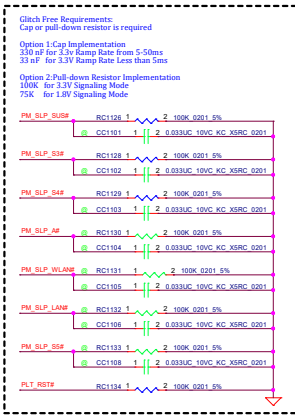
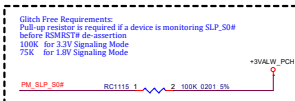
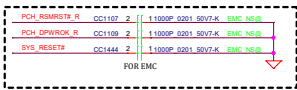
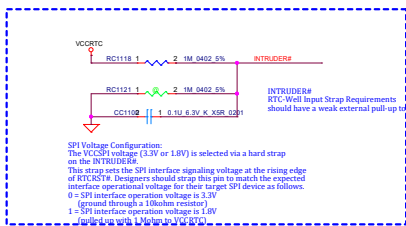
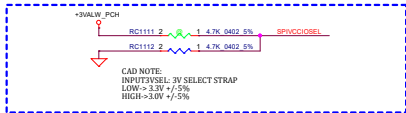
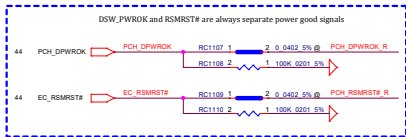


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Title		JTAG/AUDIO/SDIO/GPI	
Rev		B545A/B555A	
Date		Monday, November 12, 2018	
Sheet		8 of 88	









VDDQ_CPU :

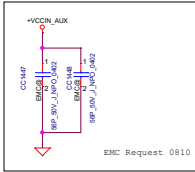
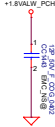
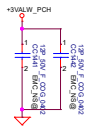
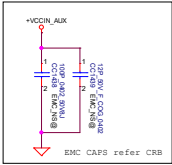
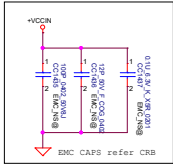
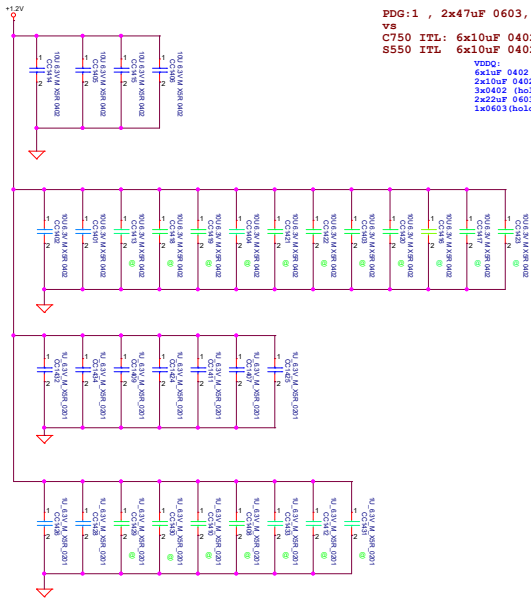
FDG:1 , 2x47uF 0603, 8x10uF 0402, 8x1uF 0402,

Vu

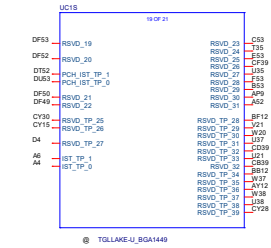
C750 ITL: 6x10uF 0402, 3x1uF 0402,10x1uF 0201,Reserve 8x10uF 0402,7x1uF 0201

S550 ITL: 6x10uF 0402, 9x1uF 0201 Reserve 11x10uF 0402, 7x1uF 0201

VDDQ:
5x1uF 0402 Back Outer row
2x10uF 0402 back Outer row
3x0402 (holder) back Outer row
2x22uF 0603 (ESD/MM need)
1x0603(holder)

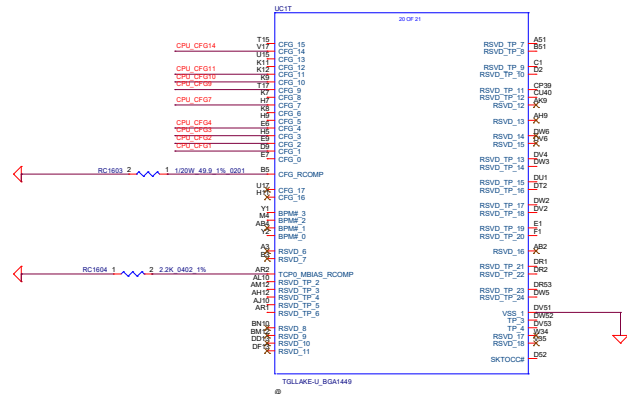


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Doc No	Document Name	RS45A/RS55A	Rev	0.1
Date	Monday, November 05, 2018	Sheet	14	of 89

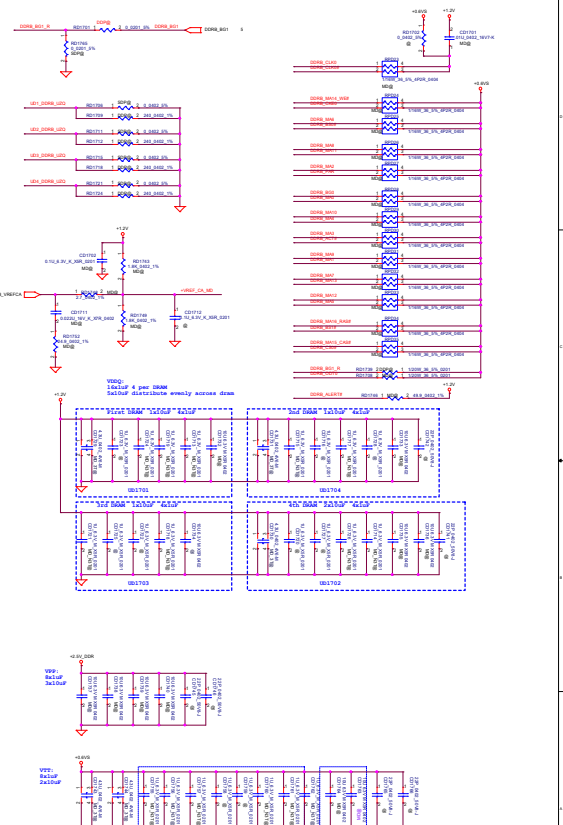


Pin Name	Strap Description	Configuration	Default Value
CPQ[0]	RSVD	None	
CPQ[3..1]	RSVD	Pull-up to VCCIO	1kOhm
CPQ[4]	eDP enable strap 1 = Enabled 0 = Enabled	Pull-up to VCCIO / Pull-down Platform design dependent	1kOhm
CPQ[6..5]	RSVD	None	
CPQ[7]	PEG deferred link training = (Geforce) PEG Train immediately following RESET# de-assertion 0 = PEG Wait for BIOS for training.	Pull-up to VCCIO / Pull-down Platform design dependent	1kOhm
CPQ[8]	RSVD	None	
CPQ[11..9]	RSVD	Pull-up to VCCIO	1kOhm
CPQ[13..12]	RSVD	None	
CPQ[14]	PEG60 Lane Reversal 1 = Normal(Default) 0 = Reversed	Pull-up to VCCIO / Pull-down Platform design dependent	1kOhm
CPQ[17..15]	RSVD	None	

Bifurcation	CFG Signals	Lanes			
	CFG [14]	0	1	2	3
1x4	1	0	1	2	3
1x4(Reversed)	0	3	2	1	0



TGLAKE-U_BGA1441

[illegible]

N16x GPIO

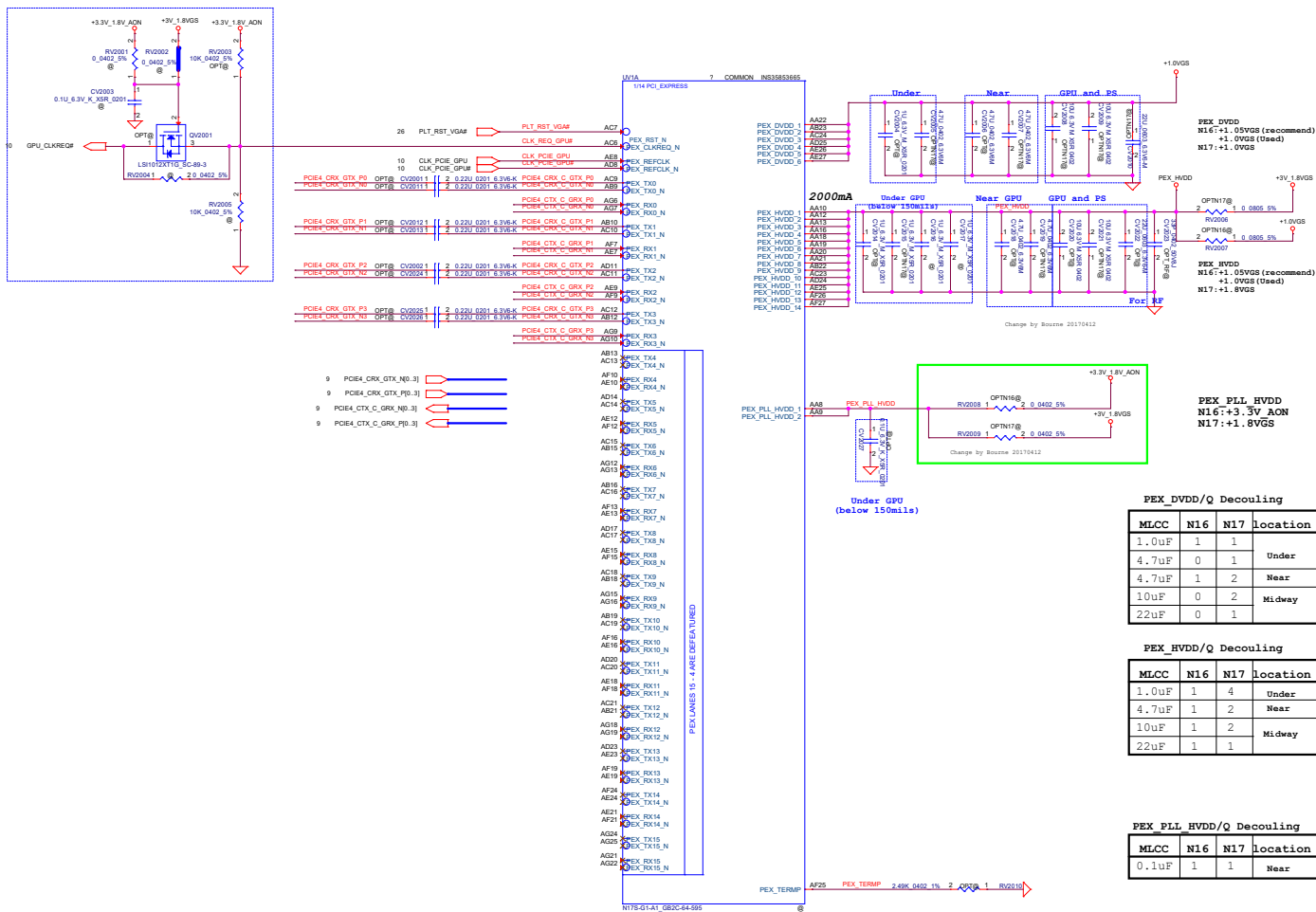
GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

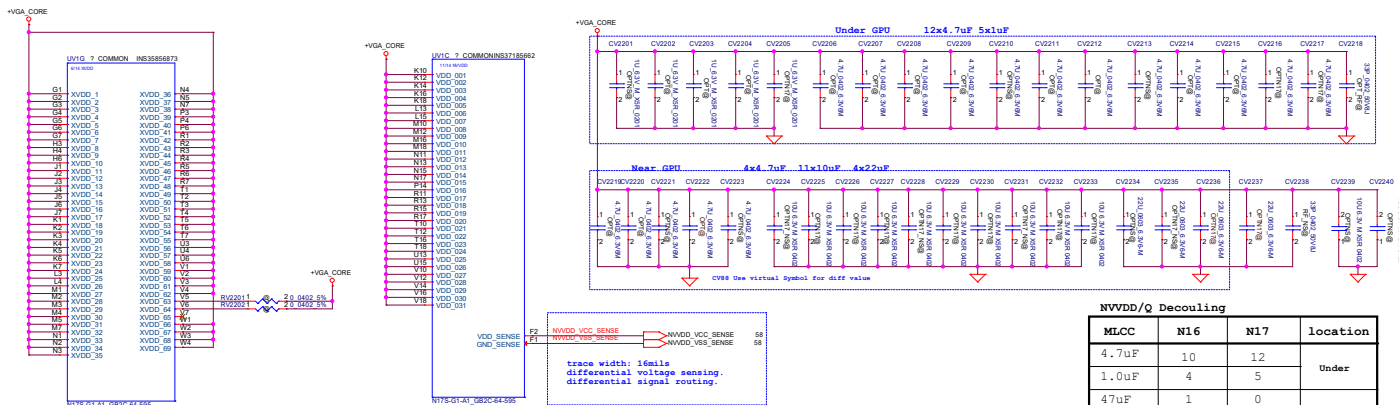
Products	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		I _{OPV} (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SORJ_EXPOSED	SORJ_EXPOSED	SORJ_EXPOSED	SORJ_EXPOSED
ROM_S1	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	+3VGS	DEVID_SEL	PCIe_CFG	SMB_ALTV_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kOhm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

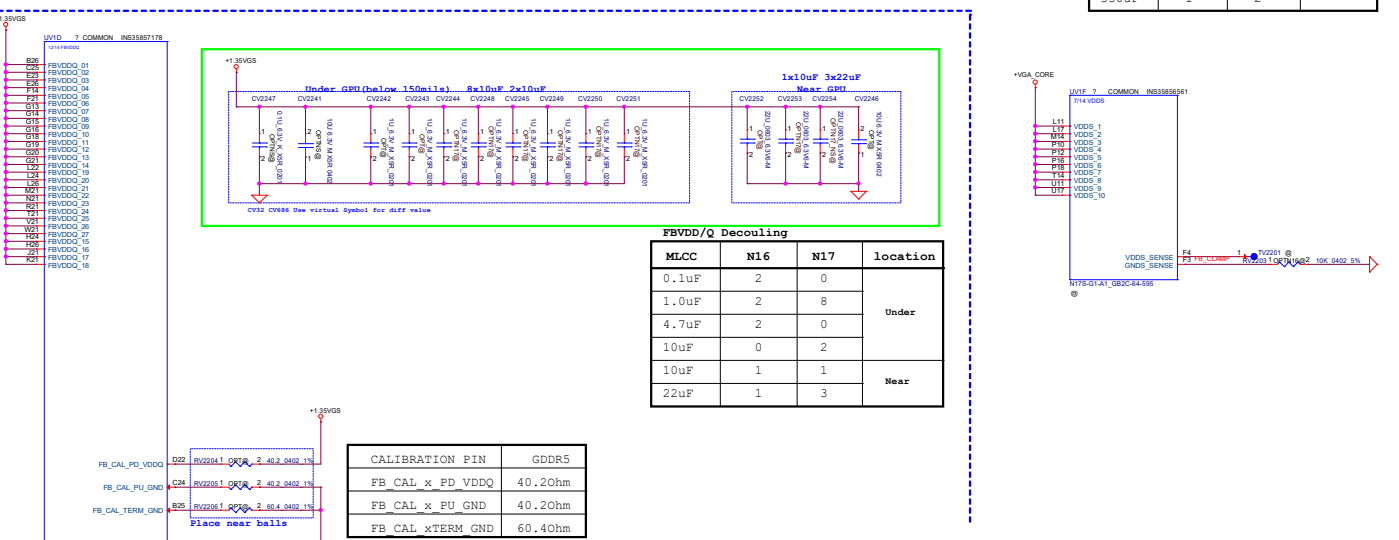


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Issued Date				Deciphered Date				GPU_PCIE Interface			
2015/08/20				2016/08/20				LCFC			
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				Date				Monday, November 22, 2015			



NVDD/Q Decoupling

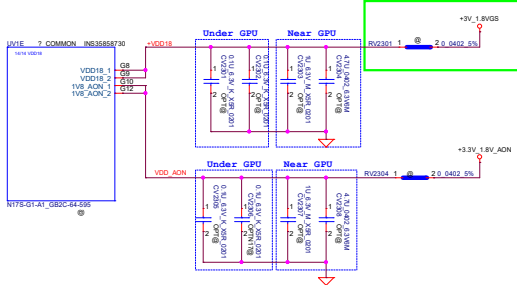
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	Near
10uF	0	2	
10uF	1	1	
22uF	1	3	

CALIBRATION PIN	GDDR5
FB_CAL_X PD VDDQ	40.2Ohm
FB_CAL_X PU GND	40.2Ohm
FB_CAL_XTERM GND	60.40hm



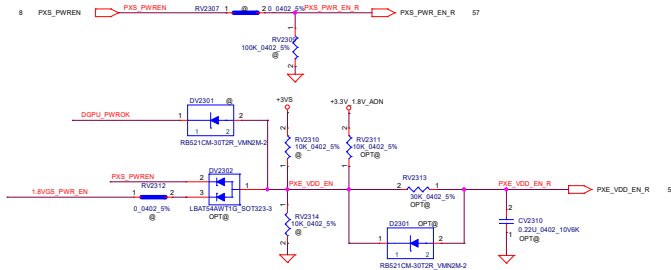
N16 3V3_MAIN(N17 VDD_18) Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	Near

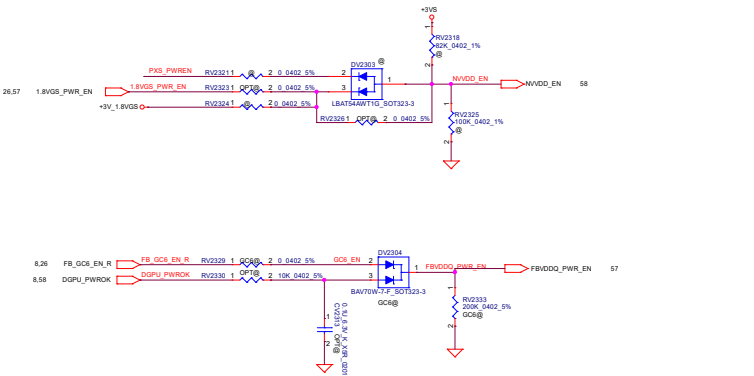
N16 3V3_AON(N17 1V8_AON) Decoupling

MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	Near

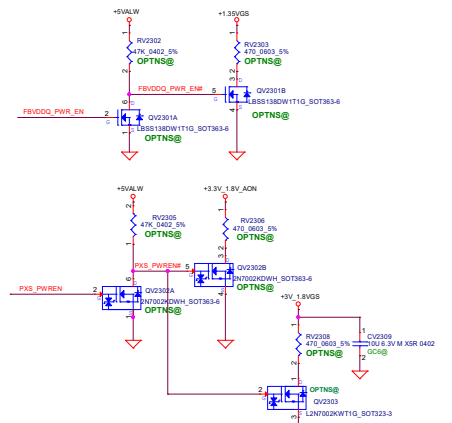
PXE_VDD & 1V8_AON



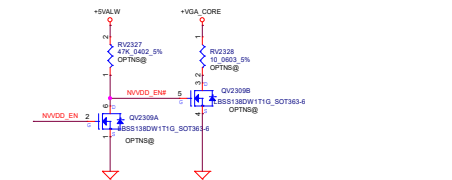
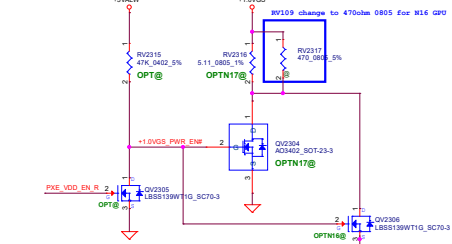
+1.8VG_AON TO +1.8VGS



Discharge



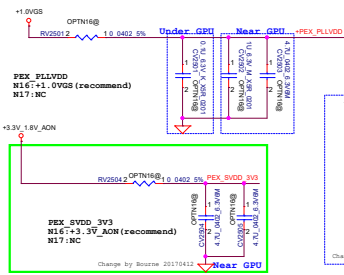
RV2316 电阻拟料号, N16=470 ohm, N17=5.11 ohm



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Doc Number	RS45A/RS55A		Rev
Doc	Monday, November 12, 2015	Sheet	22 of 88

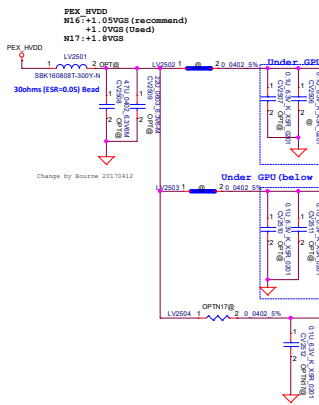
PEX_PLLVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	Near



PEX_SVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	2	NA	Near



XS_PLLVDD/Q Decoupling

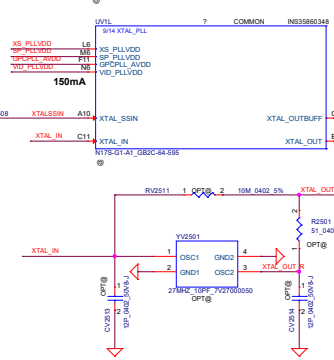
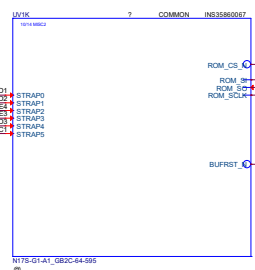
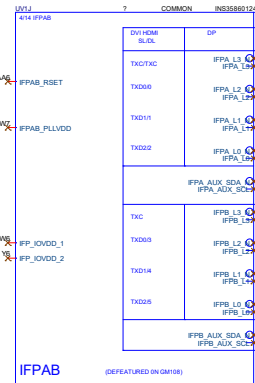
MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

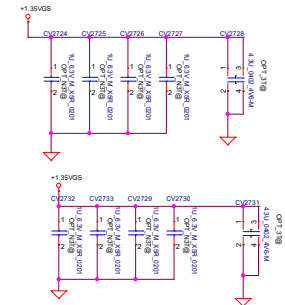
SP_PLLVDD & VID_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	Near

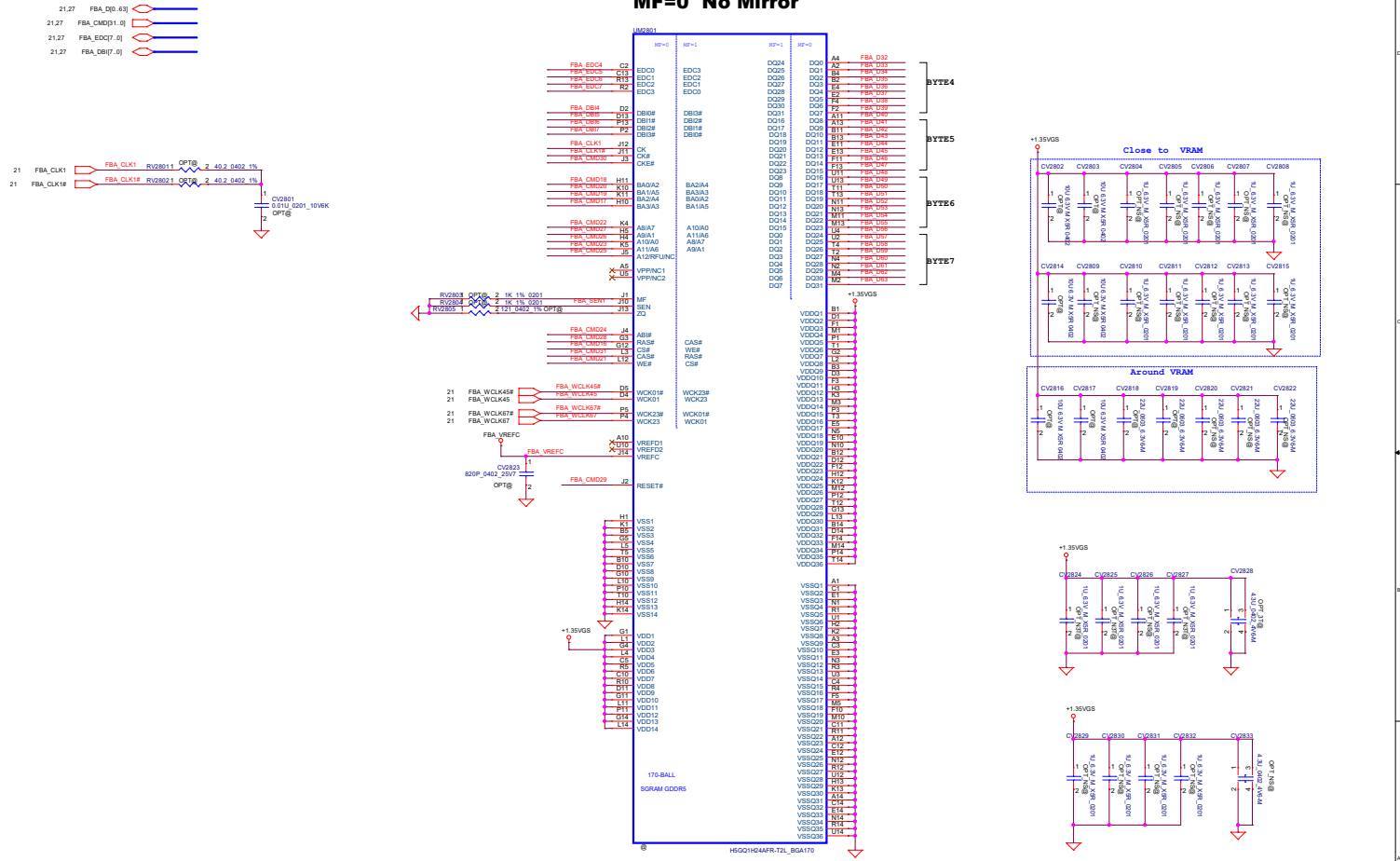
GPCPLL_AVDD/Q Decoupling

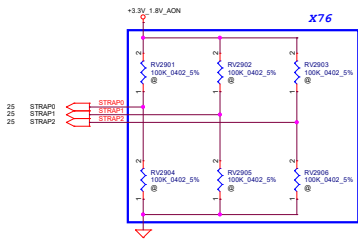
MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	Near



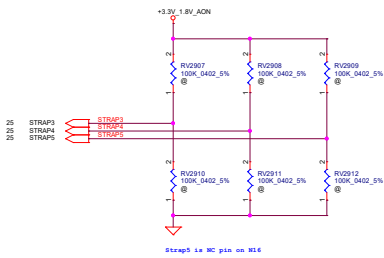
MF=0 No Mirror

MF=0 No Mirror



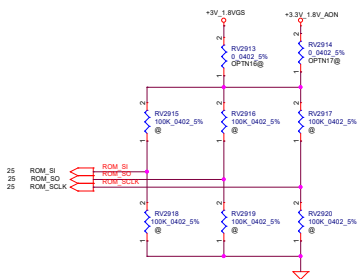


GPU	FB Memory (GDDR5)	RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	X4G80325FB-8C28	0(0x0000)	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	H
	Hynix 8Gb	H5QC8H24MJR-80C	2(0x0010)	L	L



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

- 1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE
- 1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL
- 1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER
- 1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

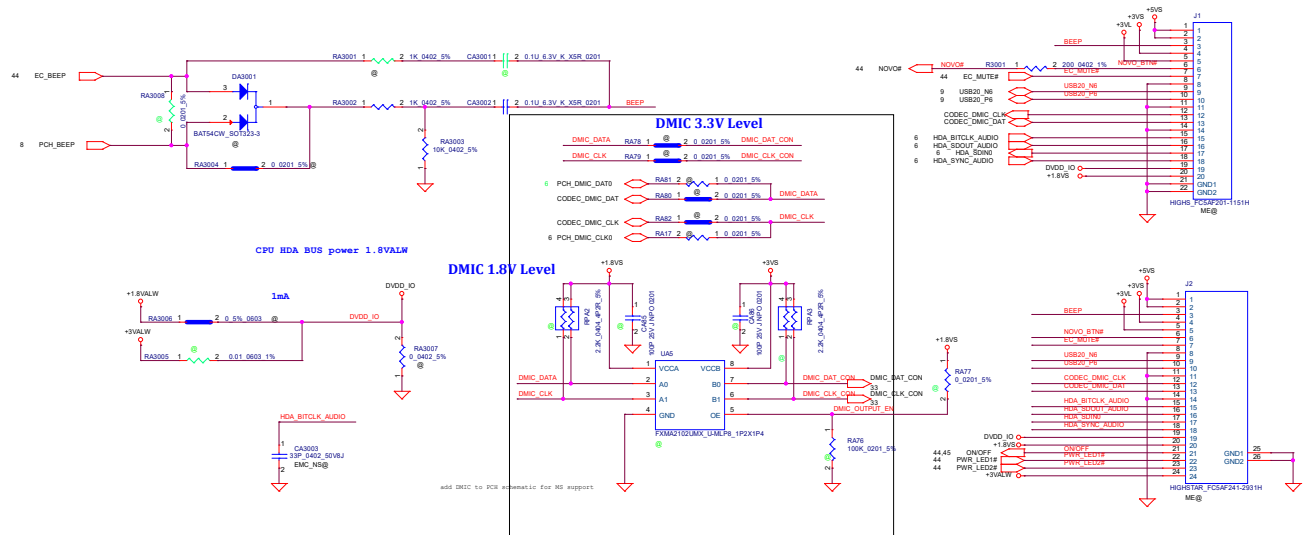
1:ENABLE 0:DISABLE
SOR0/1/2/3 DISABLE


DEVID_SEL	
0	(Default)
1	


PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
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1	0x9C (Multi-GPU usage)

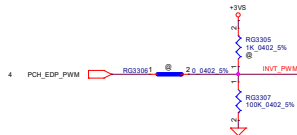
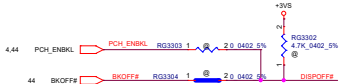
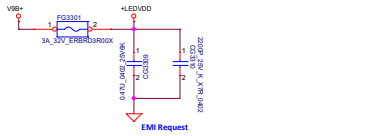
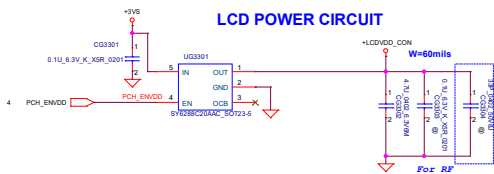
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1	VGA Device (Default)



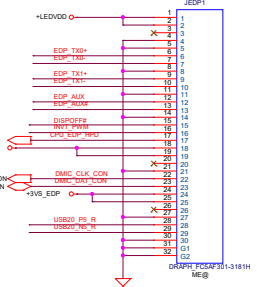
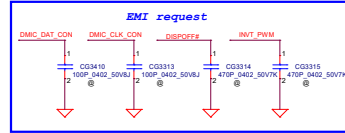
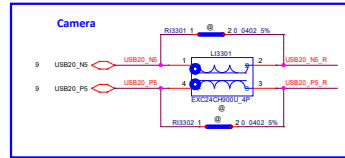
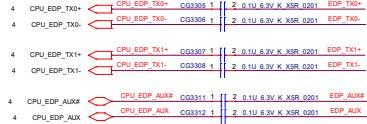
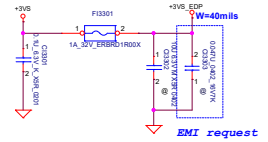
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			Scale	Monday, November 12, 2007 Sheet 02 of 00	

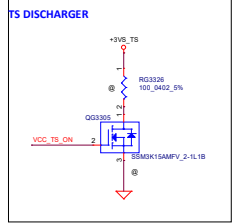
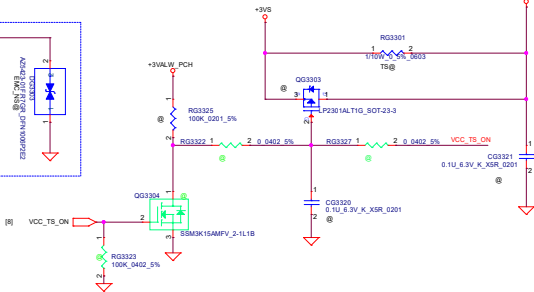
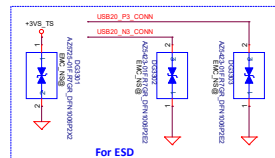
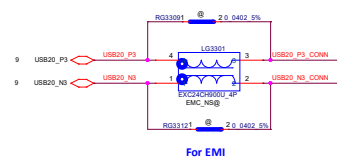
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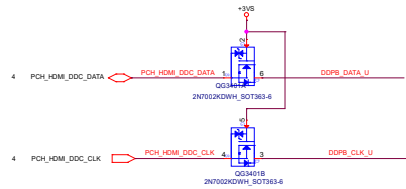
CMOS Camera



Touch Screen



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Issued Date	2015/08/20	Deciphered Date	2016/08/20	eDP/CAMERA.	
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Date	Monday, November 02, 2015			Sheet	55 of 55



1.8V

RG3425 2 1 0.0452_0%

RG3405 1 2 0.0452_0%

1M_0402 1

RG3403 1 2 0.0452_0%

LSI10121114_3C-89-3

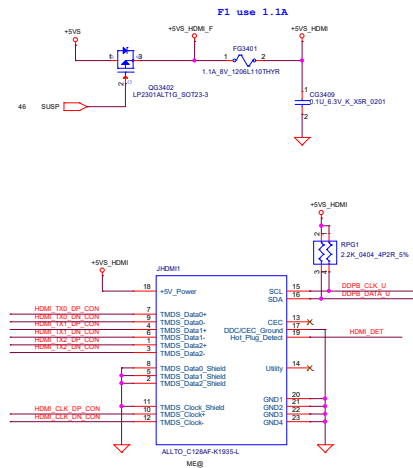
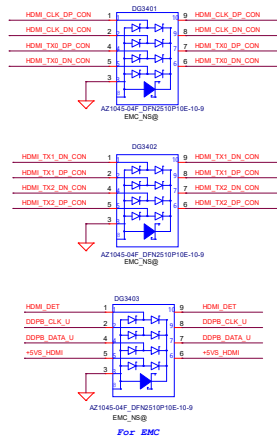
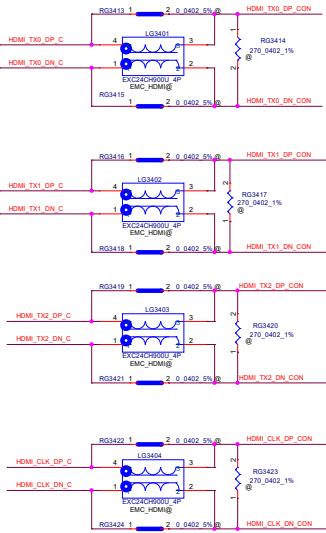
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May 06 2017 02:12:12 12:03:27



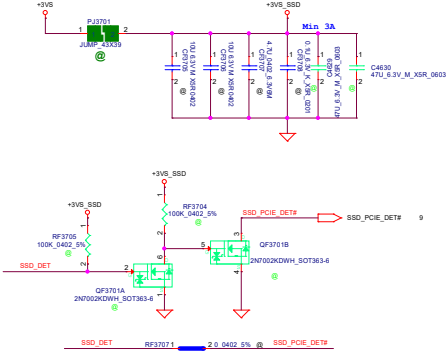
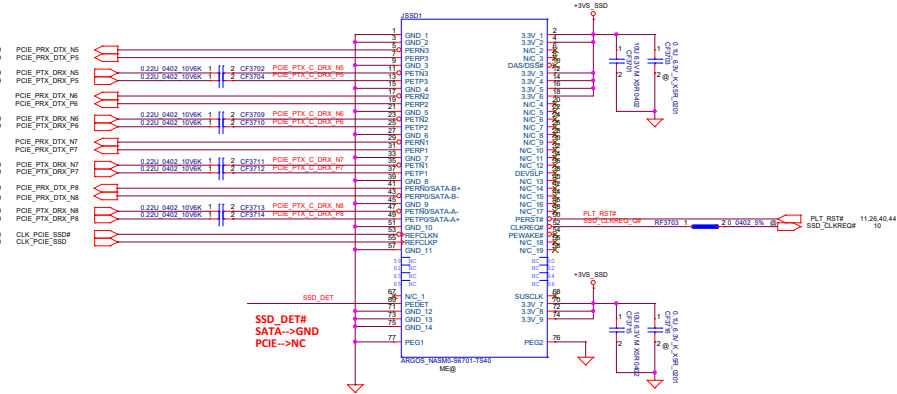
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			Date	Monday, September 12, 2016
			Sheet	35 of 80

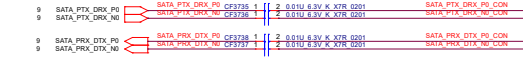


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S/N			Document Number	RS45A/RS55A
Date			Monday, November 02, 2005	Sheet 06 of 06

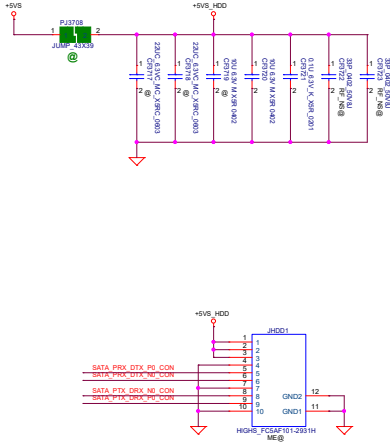
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SATA

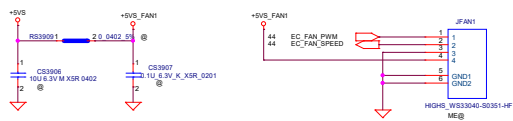
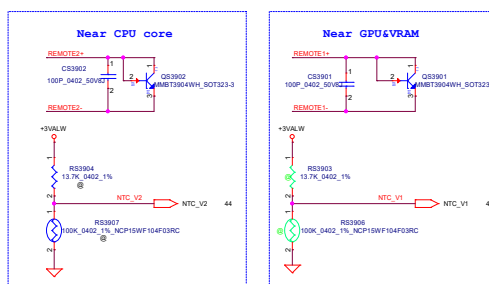


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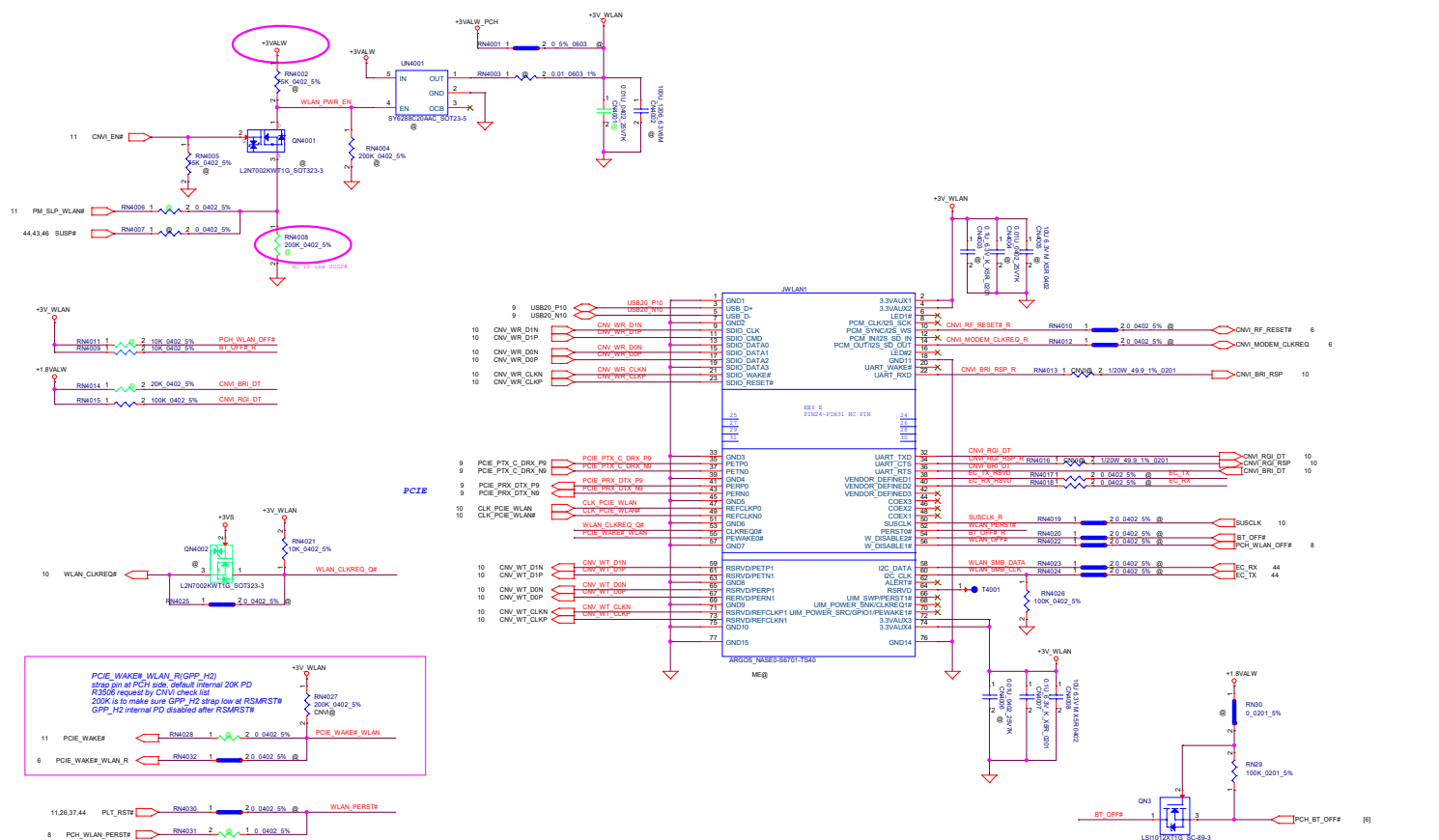
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Date			Monday, November 02, 2005	Sheet 06 of 06



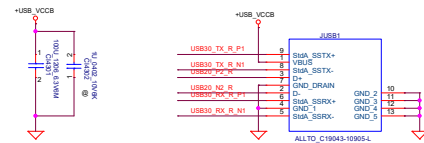
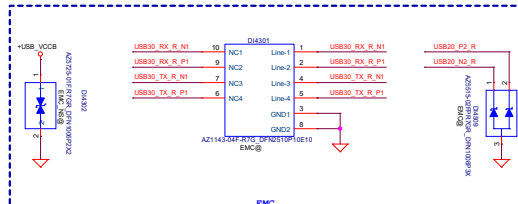
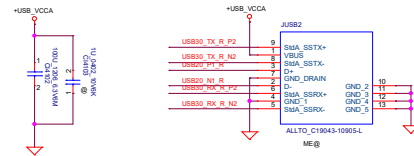
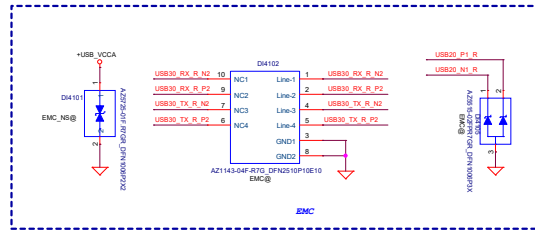
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Issued Date	2016/08/16	Deciphered Date	2017/08/15		
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Date	Monday, November 13, 2017		Page	13	of 45



Mini-Express Card(WLAN/WiMAX)



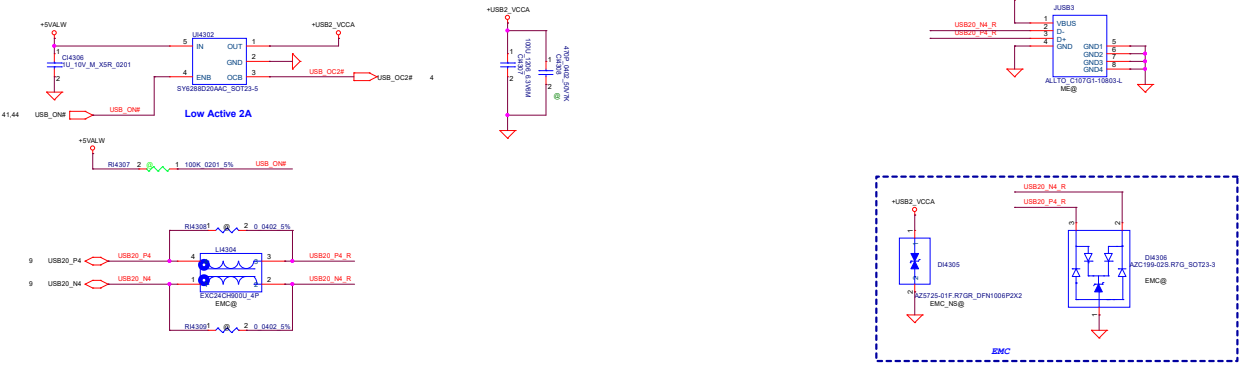
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					Monday, November 15, 2015	
					Sheet 50 of 50	

USB3.0 Port2

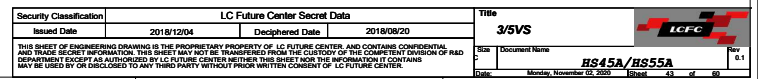


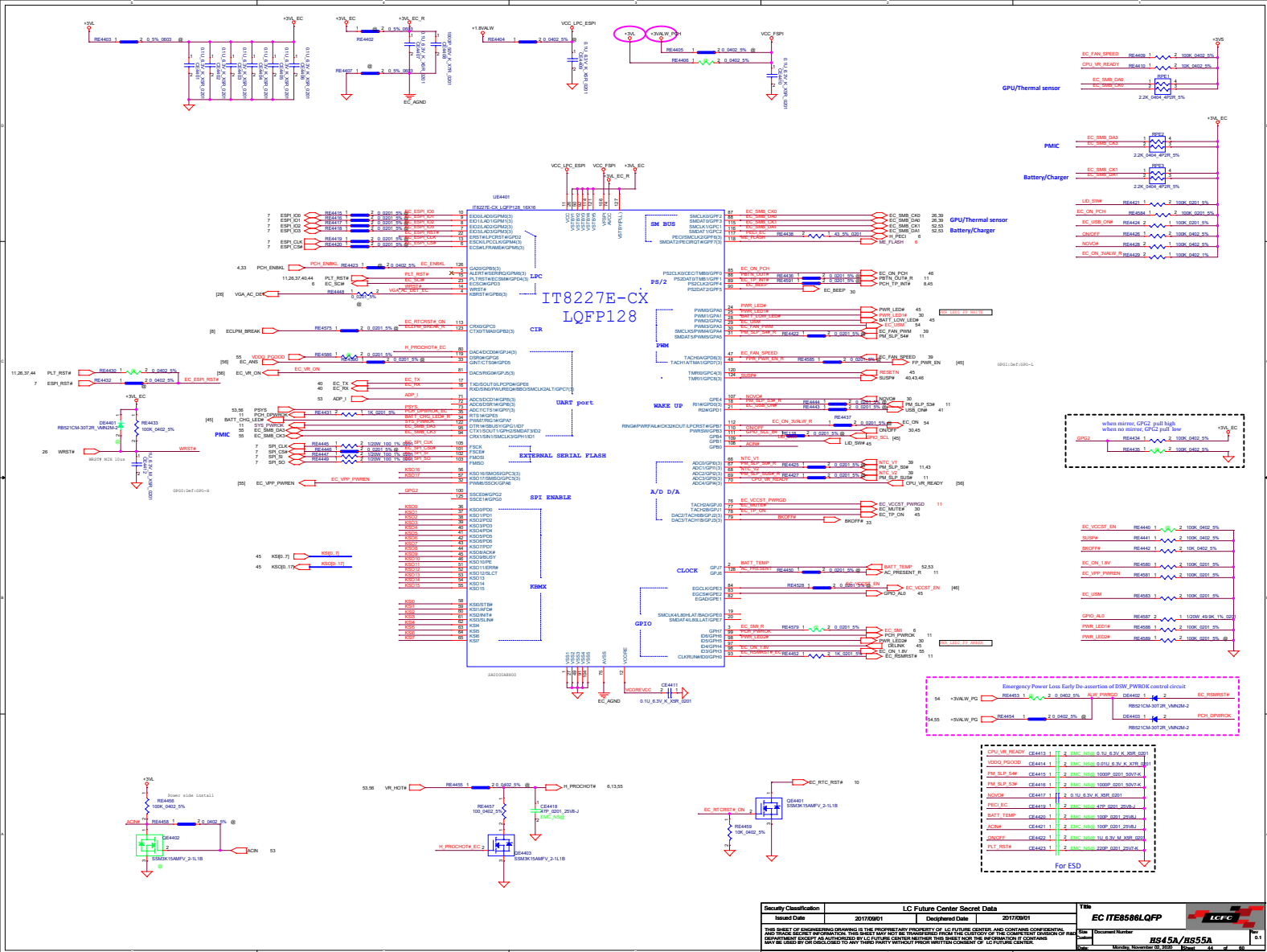
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USB2.0 PORT x1



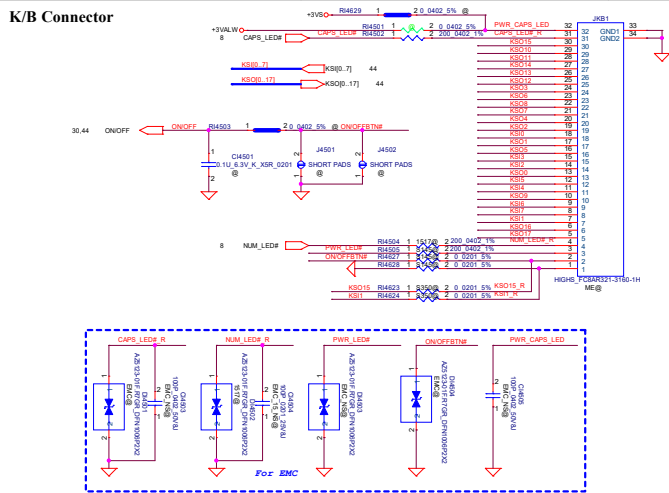
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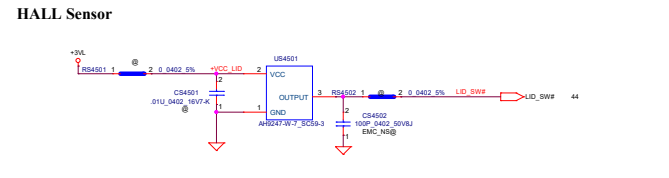


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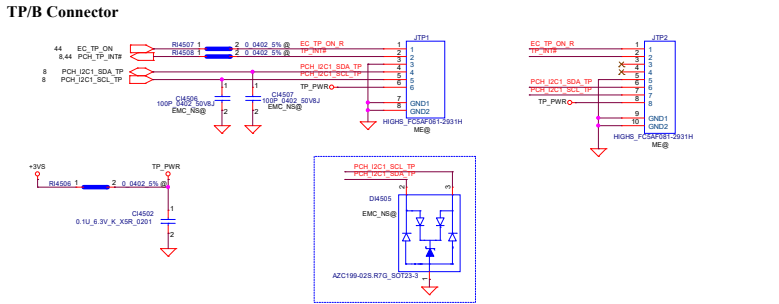
K/B Connector



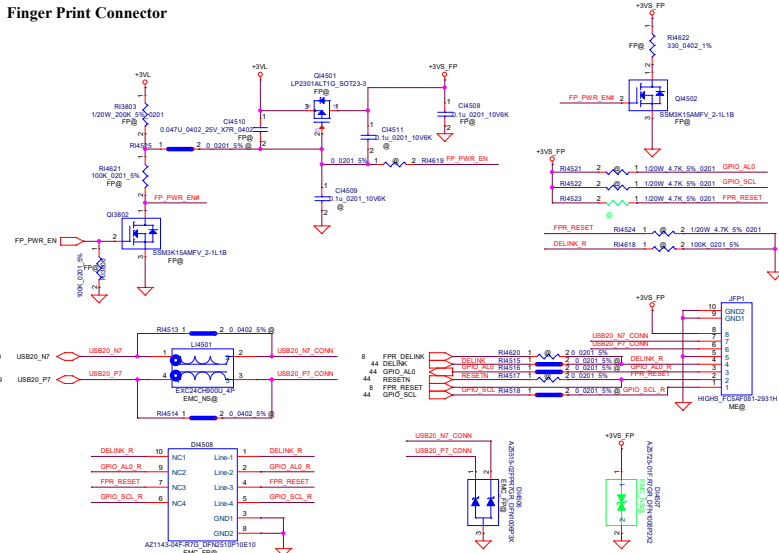
HALL Sensor




TP/B Connector

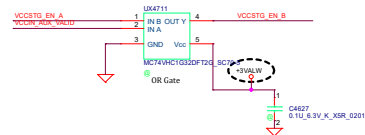
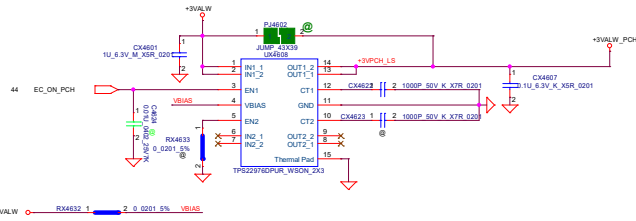


Finger Print Connector

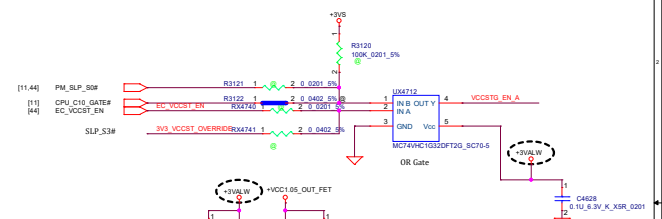
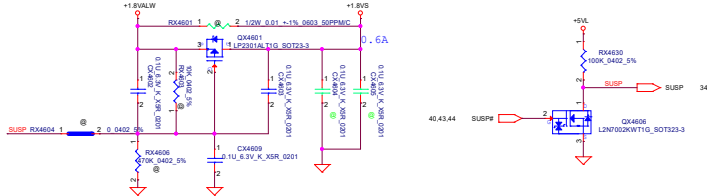


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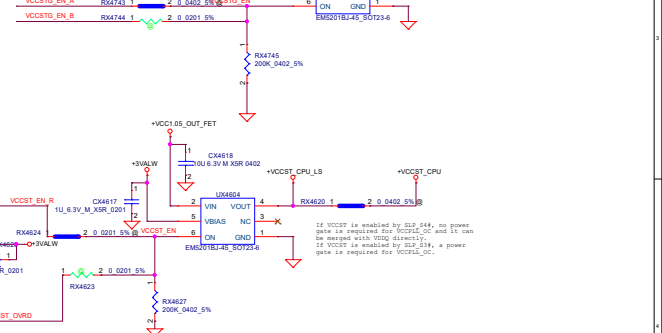
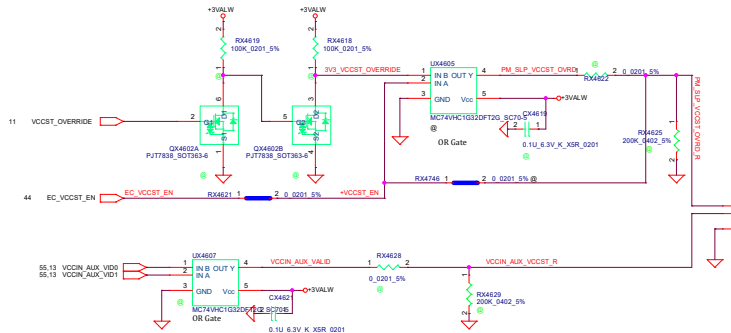
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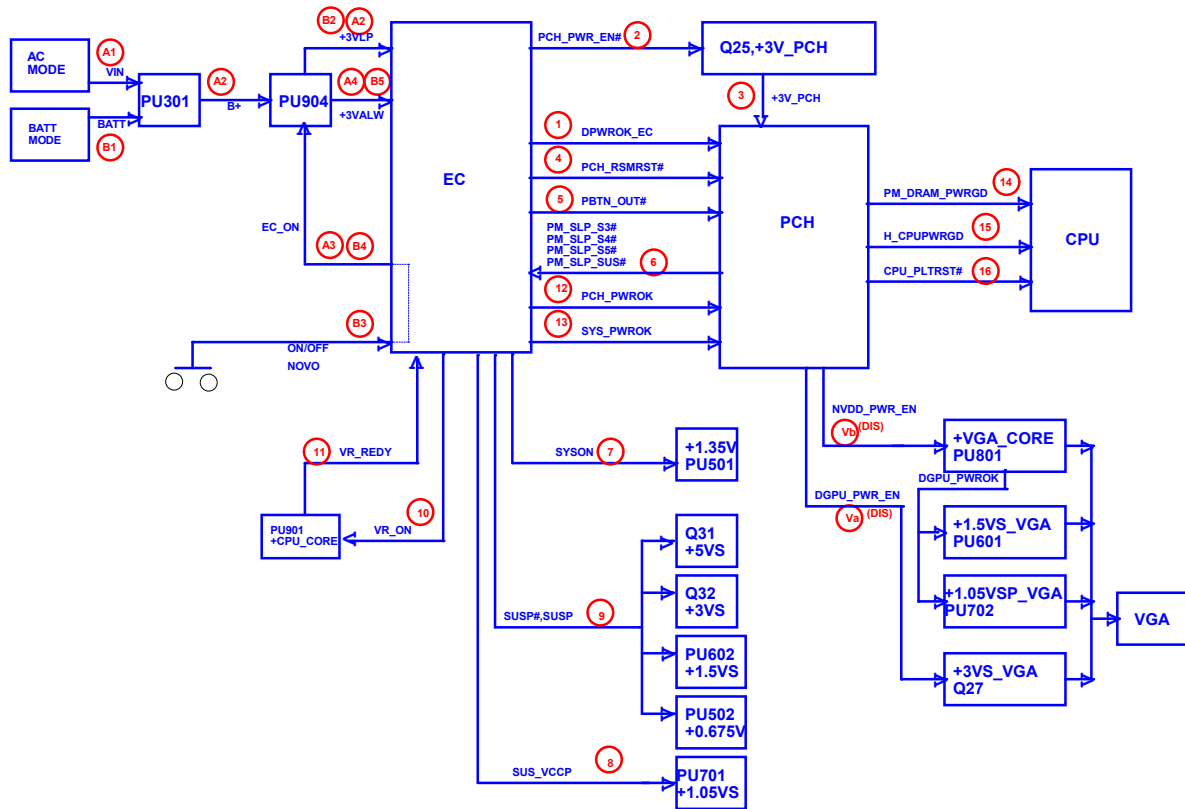
+1.8VALW to +1.8VS



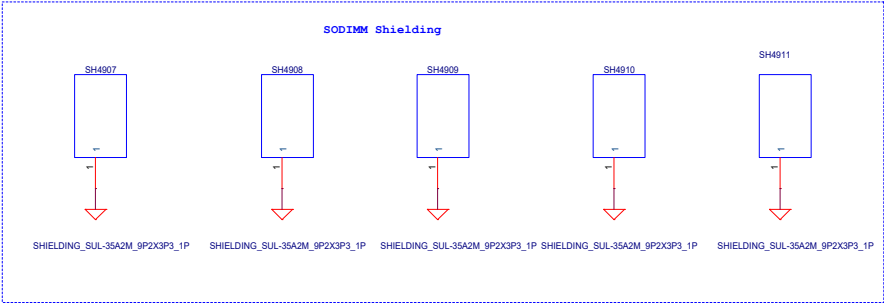
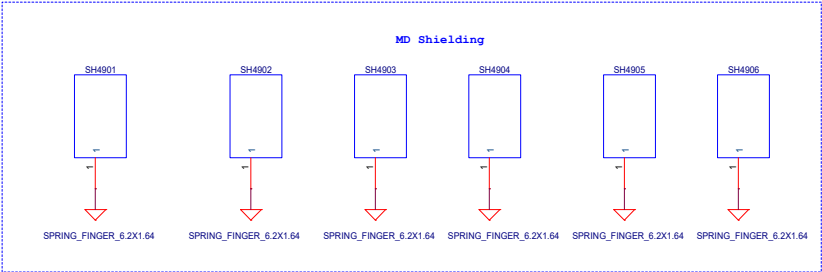
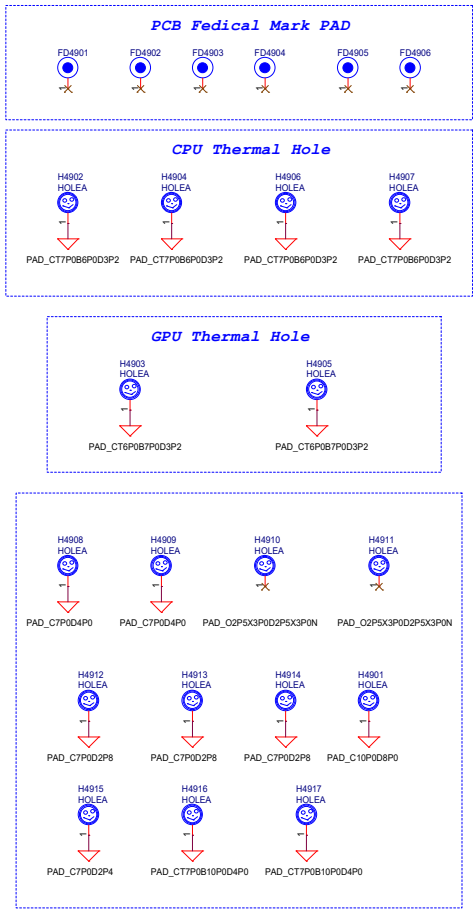
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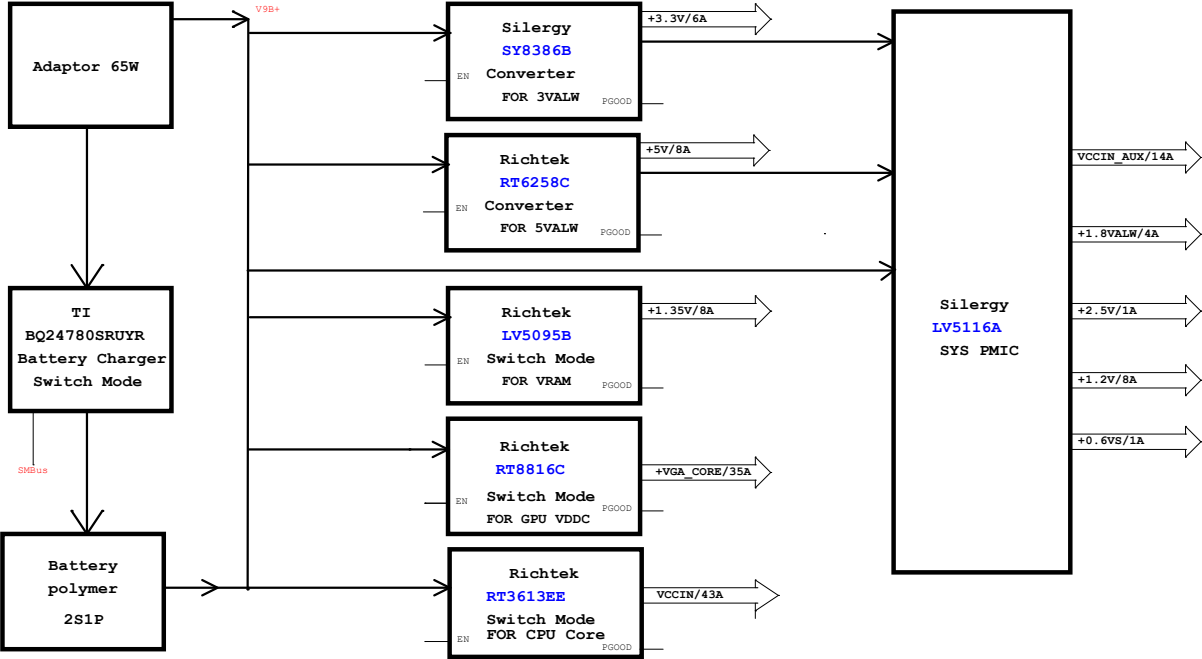
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				RS45A/RS55A	
				Monday, November 02, 2005	Sheet 56 of 60



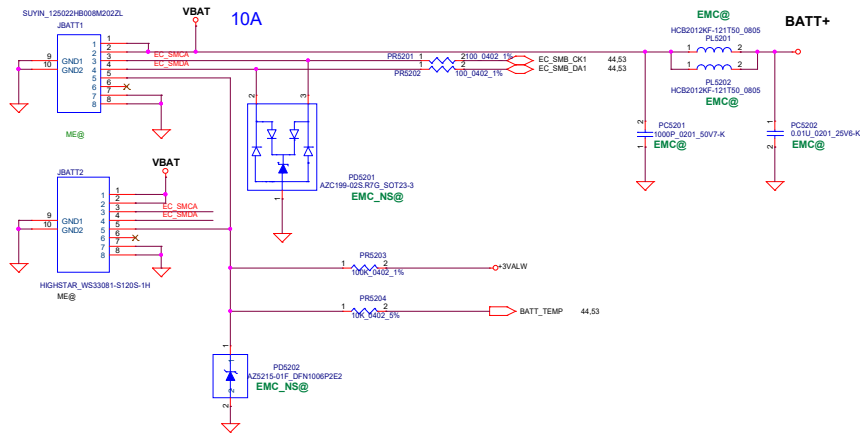
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											HS45A/HS55A	0.1
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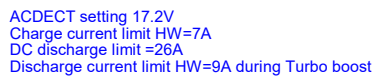



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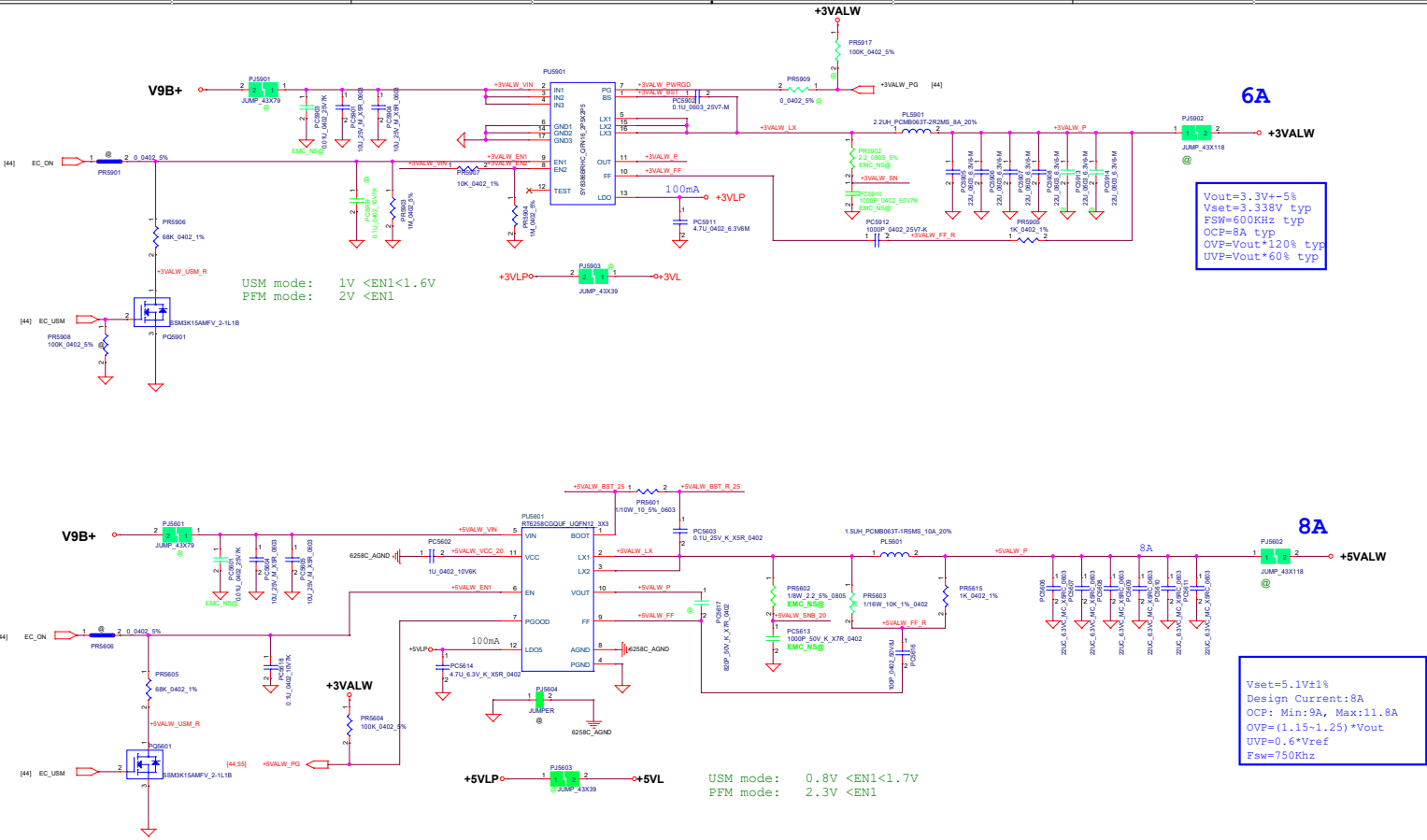


2S1P polymer battery
voltage level: +5.5V ~
8.8 V

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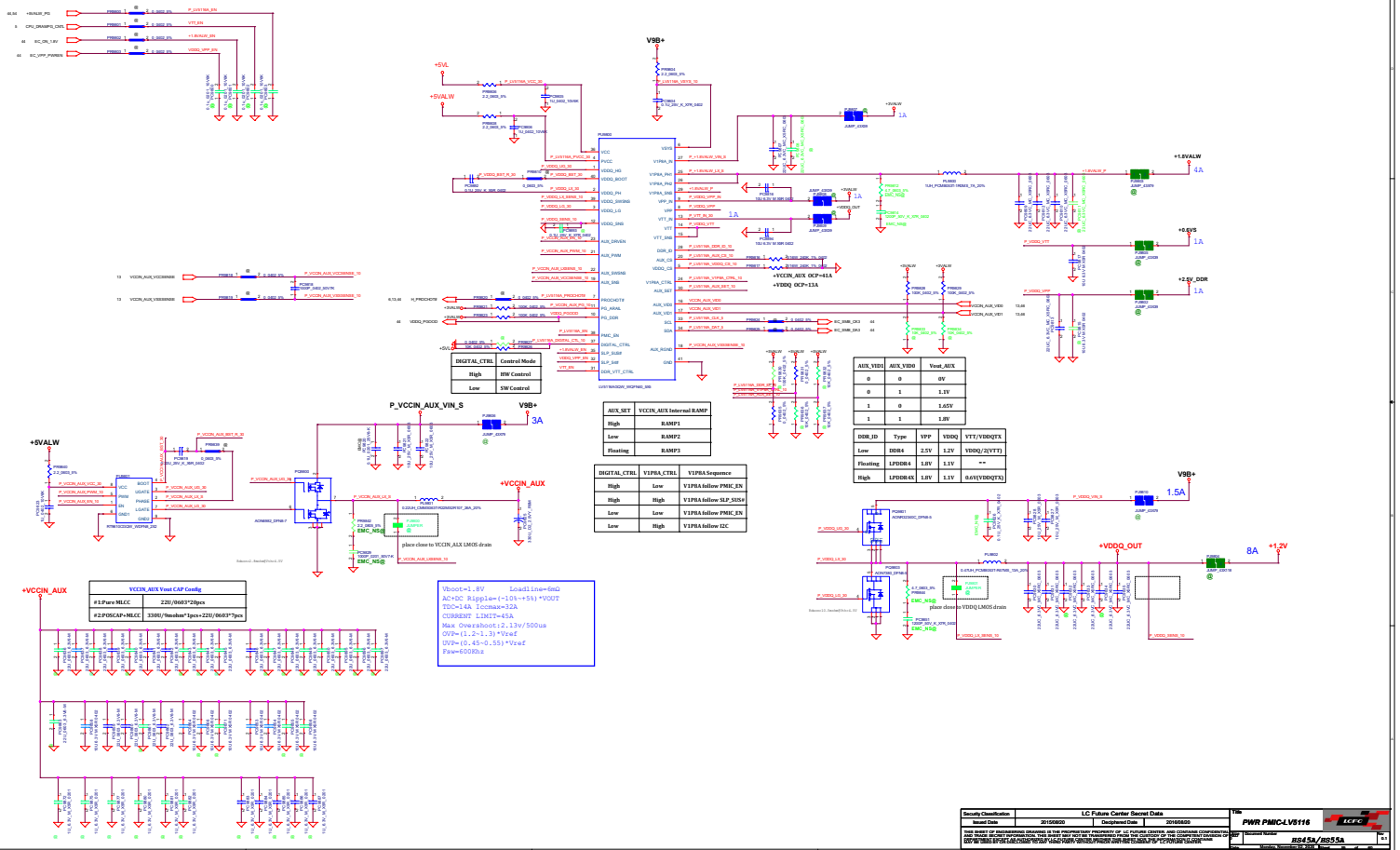


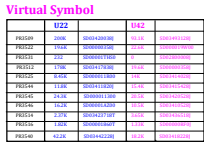
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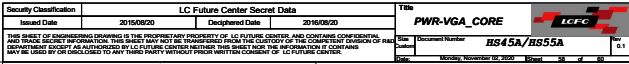
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				HS45A/HS55A	0.1
				Date	Monday, November 02, 2020
				Sheet	94 of 99


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[illegible]

RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



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